Using MOSFETs for Synchronous Rectification

The use of MOSFETs to replace diodes to reduce the voltage drop and hence increase efficiency in DC DC conversion circuits is a concept that is widely used due to the performance of today's MOSFETs. The fact that vertical MOSFETs are bi-directional and feature an internal diode makes them ideally suited for this application as the device operates as a diode with V_{GS}= 0V, so commutation can be left to the PN diode and gate drive timing is not critical to the nanosecond level. However there are many nuances that can have a large effect on efficiency and device selection.

Concept

The concept relies on the fact that MOSFETs can conduct current in either direction. The inherent diode also adds to the simplicity of a synchronous rectifier circuit.

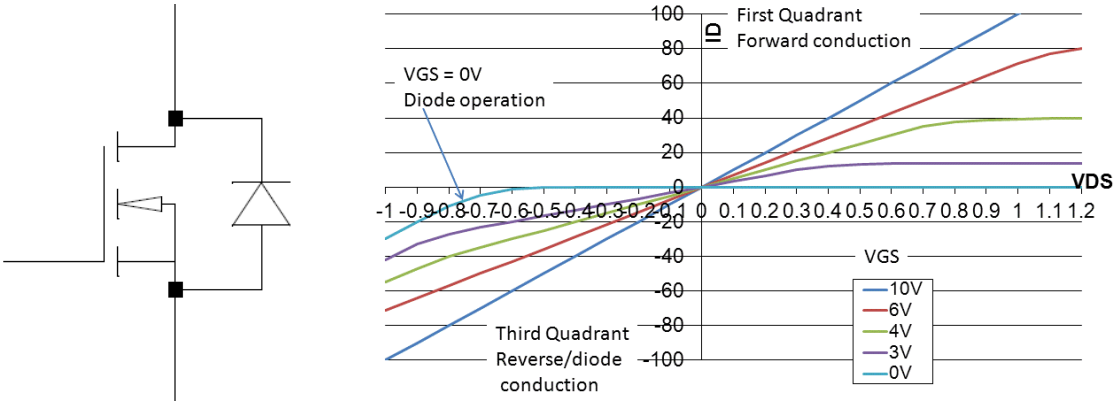


Figure 1.

MOSFET Symbol Showing the Inherent diode and I_D vs V_{DS} Characteristics showing Third Quadrant Operation

A simple example of a synchronous rectifier is an N channel MOSFET used for reverse battery protection, using the MOSFET on the ground side for simplicity:

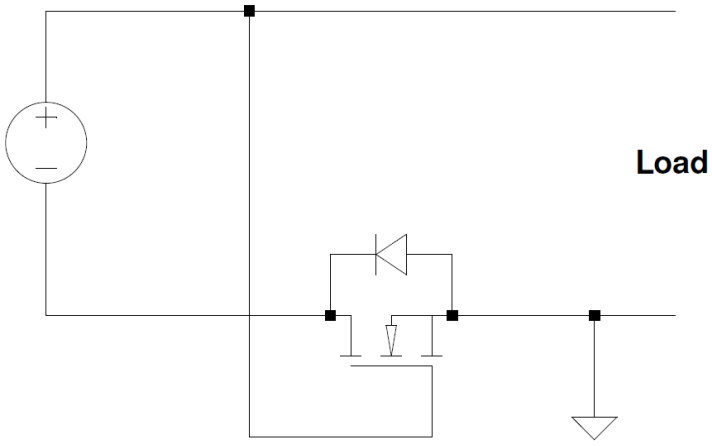


Figure 2. Reverse Battery Protection Circuit

The diode ensures that the Source is at nearly the same potential as the Drain and therefore approximately the whole input voltage is applied gate to source and the MOSFET turns on and the drop over the drain to source is then reduced.

It is them a simple step to a synchronous rectifier pair on the secondary of say a flyback converter.

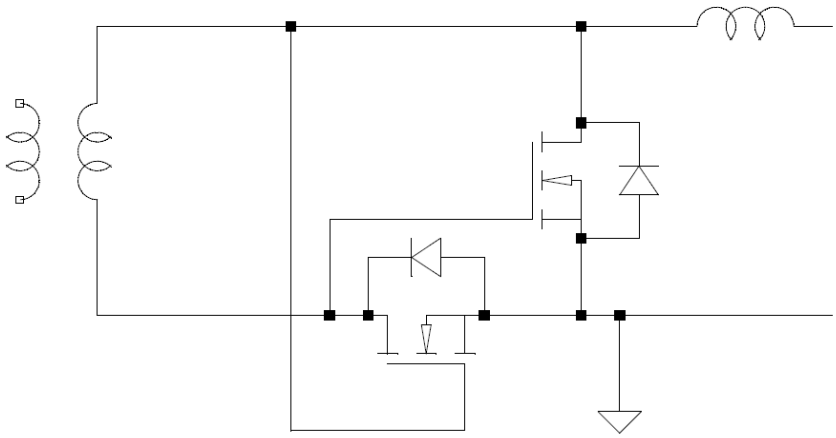


Figure 3.

Cross Coupled MOSFETs on the Secondary Side of a DC DC converter

The power stroke MOSFET operates in exactly the same manner as the reverse battery protection and a freewheel MOSFET is added, driven whenever there is a positive voltage over the power stroke MOSFET. This type of circuit has limited feasible applications however since the output voltage and primary power stroke secondary voltage must be high enough to ensure low on-resistance but not higher than the 16V operating specification of most MOSFETs. Clamps can be added to ensure V_{GS} max is not exceeded.

Dead time

The cross coupled pair of MOSFETs in Figure 3 begin to raise several of the downsides of synchronous rectification. Although theoretically impossible as drawn in Figure 3, what happens if there is some residual V_{GS} on the MOSFET when it is supposed to have turned off already, and the other MOSFET begins to turn on? Fortunately the inherent diode can be put to use to do the commutation as long as both MOSFETs are not enhanced at the moment of commutation. In simple cross coupled MOSFETs adding a resistor to slow down turn on, bypassed with a diode to ensure fast turn off can be used to reduce the chance of both diodes being on at the same time.

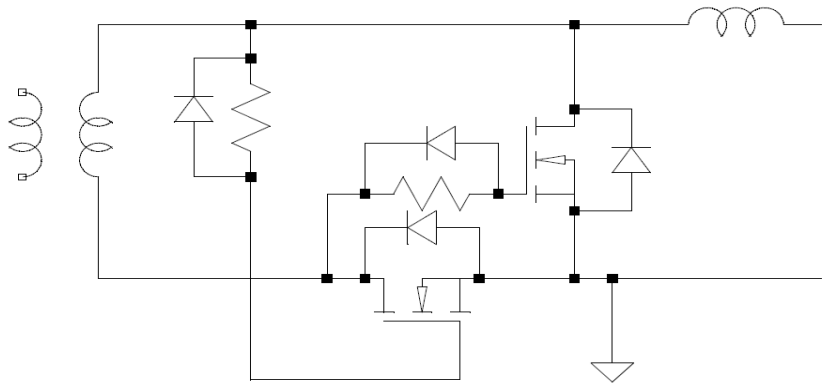


Figure 4. Implementation of Dead Time**.** Resistors and diodes added to reduce the chance of MOSFETs having V_{GS} applied when the diode should be off. The result is fast turn off, slow turn on.

This circuit begins to show an important fact: commutation is best handled by the PN diode, and therefore strong gate drive for fast turn on is not needed and is often a detriment, not a benefit. As can be seen in Figure 1, in the third quadrant, minimal gate drive voltages are not as hindering as in the first quadrant as the V_{DS} drop gets added to V_{GS}. Whatever the gate drive, the MOSFET will still be as good as a PN diode. Synchronous rectifiers are zero voltage switching; V_{DS} is minimal (a diode drop) before the MOSFET is turned on. Therefore losses are not decreased by faster gate drive. The period where both MOSFETs are off as defined by V_{GS} being below the threshold voltage is usually referred to as dead time.

Dead time is a critical parameter in high current synchronous buck converters, see Figure 5.

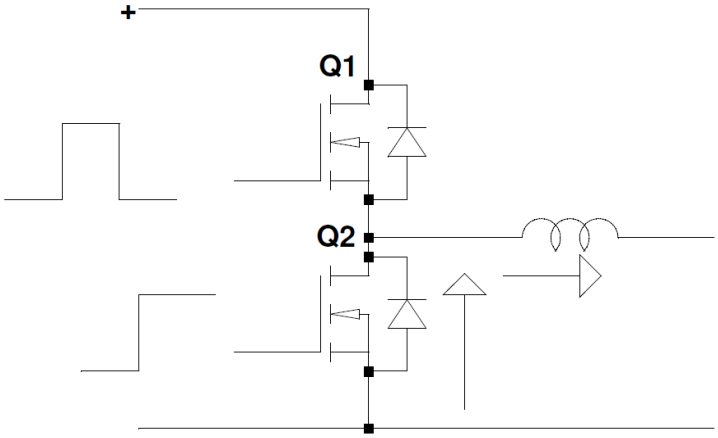


Figure 5. Synchronous Buck Converter, showing operation of bottom FET as a synchronous rectifier.

If Q2 is not fully off when Q1 is turned on, efficiency is severely compromised. To ensure the Q2 MOSFET is fully off before Q1 is turned on, dead times of ~20 to 30 ns are usually used and slow dv/dt ramp up of the gate of say ~0.2V/ns. A scope shot of a synchronous buck with bare minimum dead time is shown below. Channel 1 shows the inductor node and Channel 2 is the bottom FET gate voltage. Assuming a threshold voltage of 2V, dead time is marginal here, arguably about 10 ns. Note that V_{GS} takes about 25ns to fall from 4.5V to zero, fast gate drive is not required here for switching efficiency, however as we shall discuss later, a strong pull down may be needed to ensure the bottom FET stays off.

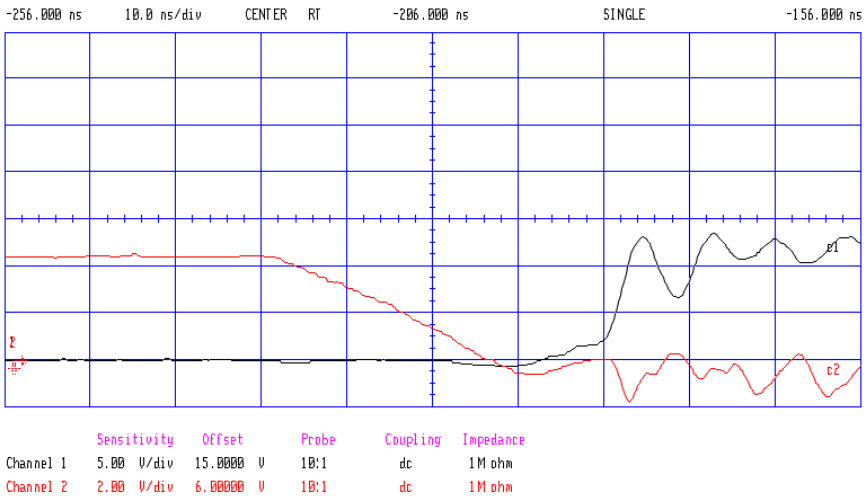


Figure 6. Scope Shot of V_{GS} for the Bottom FET of a Synchronous Buck and the Inductor Node

Excessive dead time hurts efficiency by having the diode conduct for a longer period than necessary. The diode drop can be close to 1V and the goal of using synchronous rectifiers is to reduce that voltage, but during dead time

the diode is conducting with high voltage drop. Dead time that is too short can result in the MOSFET not being fully off when the top FET turns on and therefore increase losses.

To ensure optimum dead time many ICs have an adaptive driver where V_{GS} is monitored internally and the top FET is only turned on when the V_{GS} on the bottom FET has actually fallen. However such features mean that series resistance to control V_{GS} ramp and additional buffer stages cannot be used since the IC is monitoring the voltage on its output and if that is not the same as the voltage on the gate pin, then the concept will not work properly and can actually cause simultaneous conduction.

Reverse Recovery

Using the diode for commutation is the best means of ensuring accurate commutation and is the best choice. However it does mean that there will inevitably be reverse recovery of the PN diode. This is best understood looking at the synchronous buck.

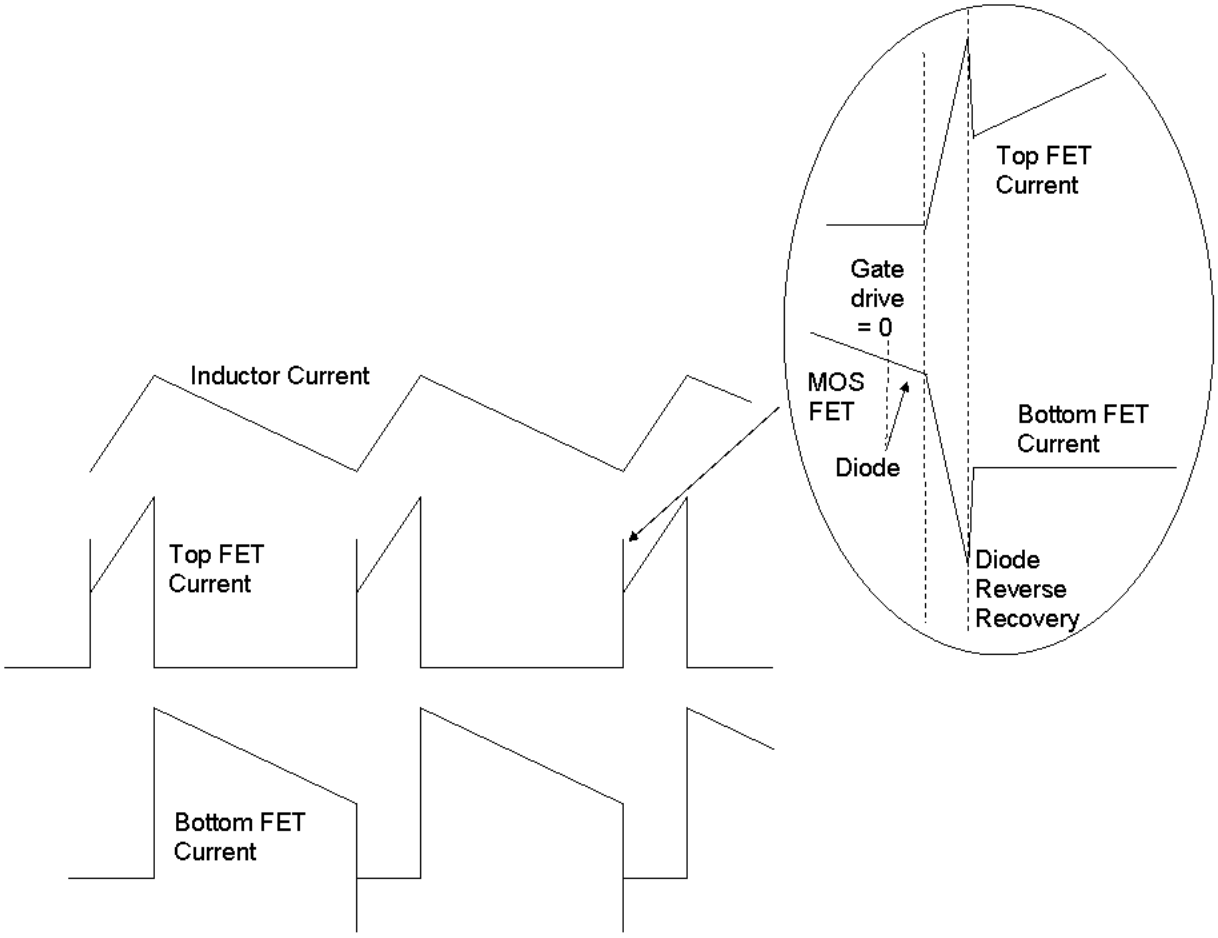


Figure 7. Reverse Recovery Current in a Synchronous Buck Converter

Reverse recovery current is a severe efficiency killer as it is current that passes through both MOSFETs (not to the load) and V_{DS} of the bottom FET is held close to zero for most of the recovery, resulting in full VIN being applied to the top FET while it is conducting load current plus reverse recovery current.

Minimizing reverse recovery current is a broad subject and one that is not very well documented. A traditional approach was to use a Schottky diode in parallel with the MOSFET so that the Schottky conducts the dead time

current, not the PN junction. However efficiency data from DC DC converters suggests that addition of a Schottky does not actually increase efficiency. Two factors are probably at play: the placement of the Schottky must be such that the current can start to flow in that path in a couple of nanoseconds, but more significant, the Schottky VF at load current must be such that the PN diode does not conduct. Therefore for a Schottky to have any positive effect, its size and cost would be prohibitive. Schottky diodes usually have a PN guard ring in the structure which means there is a PN diode in parallel with the Schottky and at currents around the rated current even the Schottky diode product will exhibit reverse recovery.

A win win method to reduce reverse recovery time is to ensure optimum dead time is used. For short (<~100ns) conduction times, reverse recovery current increases with conduction time. This has been documented by Infineon[1] and others. Short dead times also have the advantage of keeping the voltage drop low for a higher % of the cycle. It has been suggested[2] that PN diode conduction times of approximately 20 ns are optimum to reduce reverse recovery losses and ringing.

The rate of commutation (di/dt) created by the gate drive for the top FET also has an effect on reverse recovery and associated losses. Depending on layout and the characteristics of both FETs, slowing down the gate drive for the top FET can sometimes increase efficiency since stored charge (Q_{RR}) is not constant for different di/dt and higher di/dt trend to increase Q_{RR} due to lower recombination.

In transformer-based circuits such as PoE PD, dead time and reverse recovery are still factors but due to slower switching times and higher series inductance, the significance is reduced.

dv/dt Turn On, Ringing and CISS

A side effect of reverse recovery is that the voltage across the diode during the recovery process tends to be very snappy, i.e. high dv/dt over the recovering PN diode is often observed as shown in Figure 8. This high dv/dt that is a product of the recovery and of the switching time of the top fet is seen Drain to Source on the synchronous rectifier. This positive dv/dt tends to pull the gate positive with respect to the source due to Gate-Drain capacitance, which can turn on the MOSFET. The gate drive for the synchronous rectifier should be at zero or negative at this point and can help keep the MOSFET off, but due to the speed of the V_{DS} and hence V_{GS} ramp, stray inductance in the gate loop and the sheer magnitude of the positive pulse can overwhelm the pull down of the MOSFET driver.

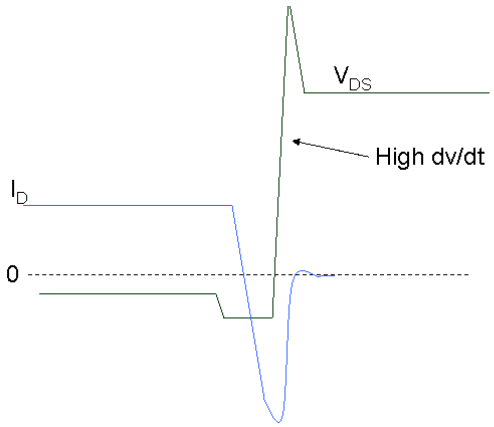
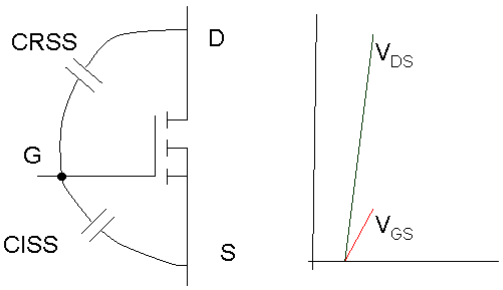


Figure 8. High dv/dt on synchronous rectifier as its diode recovers



CRSS and CISS form a capacitive divider for the Drain-Source voltage:

$$V_{GS} = V_{DS} \times \frac{CISS}{CISS + CRSS}$$

Figure 9. Capacitive Divider in a MOSFET

The MOSFET's V_{GS} must remain well below the threshold voltage for it to stay off, even 0.25 V over the threshold can result in significant losses. If a MOSFET has high R_G (the series resistance in the Gate loop inherent in the MOSFET), it is even possible for the V_{GS} voltage measured on the terminal to be below the threshold voltage but some cells in the device can be turning on. To keep V_{GS} low and the MOSFET off, six main factors play:

1. Strong pull down from the driver.
2. dv/dt as low as possible. Avoid MOSFETs with snappy diodes. Minimize parasitics.
3. The ratio of CISS to CRSS, high CISS to CRSS is better.
4. V_{IN} magnitude. Higher input voltages will produce higher V_{GS} due to the capacitive divider and once the voltage exceeds the MOSFET threshold it will begin to turn on.
5. Ensure that there is minimal inductance and no ringing in the gate drive loop of the synchronous rectifier. Avoid the worst case of having ringing and the voltage ringing up just as the positive dv/dt is applied. If the inductance in the loop is too high due to long traces, this can be mitigated by adding resistance in series with the gate to dampen any ringing that occurs.
6. Ensure that all cells of the MOSFET are fully off before V_{DS} begins to ramp and that all cells have low impedance path to the gate terminal. This is typically implemented by ensuring MOSFETs with low R_G are used and that the V_{GS} is well below the threshold.
7. Remember to check for compliance with V_{GS} maximum ratings, positive and negative.

Looking at V_{IN} and the ratio of CISS to CRSS, a typical ratio at V_{DS} = 0 (not at 15V as may be shown in the table of the datasheet) is about 5 :1 . Therefore even at input voltages of 12V, it is possible that a $V_{GS(th)}$ value of 2.0V can be exceeded. At higher V_{IN} voltages of 19V say, the likelihood is even higher. High or even added external CISS significantly reduce dv/dt turn on. Higher CISS is therefore often an asset in synchronous rectifiers.

dv/dt turn on is not so much of a common problem for transformer-based designs due to slower switching speeds, however it does occur sometimes. The addition of more resistance in series with the gate of the main PWM MOSFET or addition of a little extra CISS can usually eliminate it. However excessive V_{DS} ringing resulting in higher ratings being required is often a problem. To minimize ringing and allow use of a lower rated V_{DS} MOSFET, first ensure there is plenty of dead time and a strong V_{GS} pull down to ensure that high currents due to cross conduction are not adding to the magnitude of the ringing. Also slowing down the switching speed of the PWM MOSFET will reduce ringing and may not affect efficiency as much as may be thought. Cross conduction can increase ringing and could force use of a higher voltage synchronous rectifier.

Gate Drive

Many different ideas exist for the gate drive, but as shown already the following tips might be useful

- Always ensure there is dead time before the MOSFET should block. Fast turn off, slow turn on can produce some dead time.
- Slower turn on seems to work better than fast turn on. Being over zealous with a synchronous rectifier turn on does not improve the efficiency.
- 5V gate drive (as opposed to 10V or 12V gate drive) is usually optimum.
- Strong turn off to ensure tight dead time controls and reduce the chance of dv/dt turn on is required, however if there is excessive inductance, adding series resistance may be required to avoid ringing on the V_{GS} as it turns off.

The impact of excessive inductance in the gate drive path for the synchronous rectifier can be seen below in Figure 10. Channel 1 is the gate drive output of the IC and Channel 2 is the voltage at the gate.

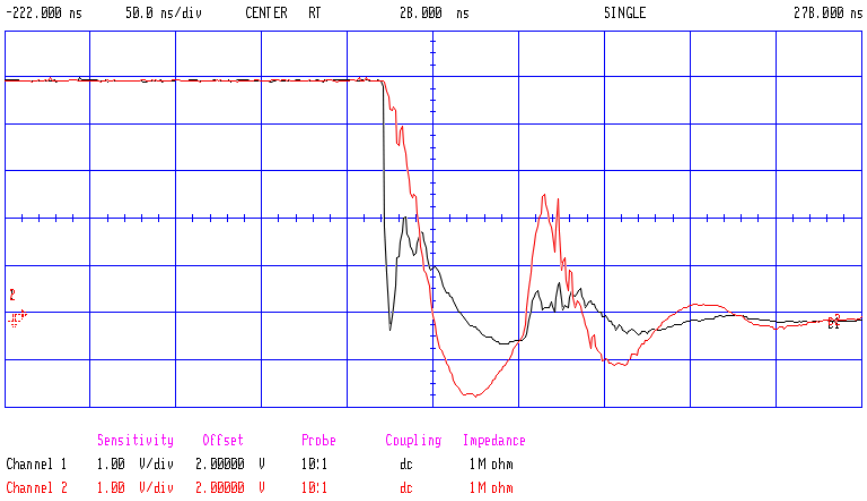


Figure 10. Impact of Excessive Trace Length and Inductance in Gate Drive.

The key relevant issue here is not the delay in turn off due to the inductance, it is the propensity for V_{GS} to ring back up to a positive value that may occur just as the dv/dt is occurring. Such ringing is corrected by putting series resistance of ~1 Ohm in series with the gate. The results are shown in Figure 11.

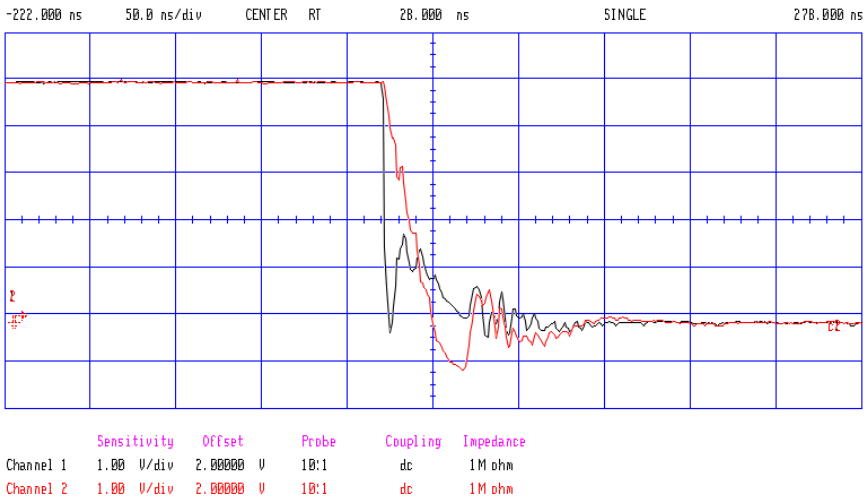


Figure 11. Impact of 1 Ohm Resistor in Series with the Gate Drive.

Turn off time is hardly affected but the positive ringing back voltage is greatly reduced. If there is significant inductance in the gate drive loop, added resistance will usually reduce losses and for some circuits, finding the exact value of resistance to add is critical to maximizing efficiency.

Losses and Device Selection

Losses in the synchronous rectifiers come from three parameters

- Gate Charge losses due to charging the gate and then discharging/dissipating the charge
- Reverse recovery losses seen elsewhere in the circuit but caused by reverse recovery of the diode
- Conduction losses

Gate charge losses are independent of load current. They are equal to the energy required to charge the capacitance multiplied by the frequency and are approximately given by :

Losses = CISS x $(V_{GS(on)})^2$ x F

Where:

CISS = Capacitance (F) at V_{DS} = 0V

$V_{GS(ON)}$ = on state gate voltage (V)

F = Switching Frequency (Hz)

Looking at say a AM7426N operating at 300KHz and 5V gate drive

Gate drive Losses = $4.5 \times 10^{-9} \times 5 \times 5 \times 300 \times 10^3$ = 34 mW

Note that at 10V gate drive, the losses would be 4X that value, and that would be a significant % of say a 10W output. Note also that if the 5V rail is derived from a LDO from a higher voltage, then the losses can be significantly higher.

Conduction losses are easily calculated if dead time is ignored:

Losses = I_{RMS}^2 x R_{DS} x Duty Cycle

Where:

I_{RMS} = RMS current through the rectifier (A)

R_{DS} = on resistance under the actual conditions (Ohms)

Using the AM7426N example and using 6 m Ohm for a warm R_{DS} and assume a RMS current of 10A at a 50% duty cycle:

Losses = 10 x 10 x 0.006 x 50% = 300mW

Note that for this case CISS losses are much smaller than conduction losses, which emphasizes that higher CISS is not always a bad thing.

Selecting the best MOSFET usually starts with the voltage rating. However selecting the optimum voltage rating may not be as simple as would seem due to the severe ringing often seen at diode commutation. Trying a

MOSFET with V_{DS} rating of 4 x the blocking voltage for a transformer secondary circuit is a starting point and then trying it in the circuit and measuring the peak voltage it sees.

Selecting the R_{DS} is a question of balancing conduction losses, cost and gate charge losses. Picking R_{DS} to give an voltage drop of 50 to 100 mV at full load taking into account the increase in R_{DS} at temperature is a reasonable starting point for transformer designs.

Conclusions

MOSFETs make synchronous rectification feasible due to the third quadrant conduction and inherent PN diode. However a successful synchronous rectifier circuit has to take into account the need for dead time, optimum gate drive voltage, gate series resistance, reverse recovery characteristics and dv/dt turn on risks. Device selection is often governed by voltage rating that is in turn governed by overshoot and ringing at diode commutation. However efficiencies higher than diode-based designs are easy to reach and with optimization, highly efficient designs are possible.

References

1. Mößlacher Christian, Guillemant Olivier. Improving Efficiency of Synchronous Rectification by Analysis of the MOSFET Power Loss Mechanism. Infineon Technologies Austria AG 2012-03-16

2. Mößlacher, Christian. Guillemant, Olivier. Simple Design Techniques for Optimizing Efficiency and Overvoltage Spike of Synchronous Rectification in DC to DC Converters Infineon Technologies Austria AG 2011-02-02